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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/273,784	03/22/1999	JOHN G. MCBRIDE	10971308-1	7570

22879 7590 04/04/2005

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EXAMINER	
PHAN, THAI Q	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/273,784	MCBRIDE, JOHN G.	
	Examiner	Art Unit	
	Thai Q. Phan	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/24/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,8,9,15 and 16* is/are rejected.

7)☒ Claim(s) *3-7,10-14 and 17-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to Applicant's Appeal dated 11/24/2004 (the "Appeal Brief").

In view of the Appeal Brief, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment f the application, appellant must exercise one of the flowing two options:

(a) file a reply under 37 CFR 1.111 (if this Office action in non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(b) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 8, 9, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Luk et al, US patent no. 5,883,814.

As per claim 1, Luk discloses a method and system for compilation of the chip design to meet performance with feature limitations similar to the claimed invention (Summary of the Invention, col. 8, lines 33-38, for example). According to Luk, the rule checking method and system for design rule verification includes means:

a computer configured to execute a rule checker program (Figs. 9, 14, col. 8, lines 33-53, col. 12, lines 21-28), wherein the design rule being checked for noise performance of an integrated circuit design having CMOS gates, gate connected in datapath or along circuit paths including static gate characteristics, transistor parameters such as transistor widths, lengths, connected in device channel, etc. (Figs. 9, 14, col. 9, lines 15-50, col. 10, lines 12-57, for example). The design rule checker program is to check transistor noises such as transient noise, noise levels, etc. for noise immunity (col. 5, lines 35-48, cols. 9-12). Luk does not expressly disclose the claimed "gate width" of the gate transistors under rule checking (DRC) program.

Practitioner in the art at the time of the invention was made would have found Luk chip design verification above would include the claimed gate width because the design rule check program checks CMOS gate parameters in the gate layout such as gate transistor width, size, etc. in determination of the gate noise immunity.

As per claim 2, Luk discloses CMOS transistor size for layout implementation including design parameters, wherein the gate transistor design parameters would include channel length, gate width, channel widths, gate terminals or pins, and the likes for logic gate design checking and noise verification as above.

As per claim 8, Luk discloses a method and system for compilation of the chip design to meet performance with feature limitations similar to the claimed invention (Summary of the Invention, col. 8, lines 33-38, for example). According to Luk, the rule checking method and system for design rule verification includes means:

Receiving input in a computer relating to characteristics of a static gate contained in the integrated circuit (Fig. 14), the gate as known in the art comprising at least two field effect transistor (MOS technology), each field effect transistor having a width, and gate characteristics (Fig. 14, col. 9, lines 40-40),

a computer configured to execute a rule checker program (Figs. 9, 14, col. 8, lines 33-53, col. 12, lines 21-28), wherein the design rule being checked for noise performance of an integrated circuit design having CMOS gates, gate connected in datapath or along circuit paths including static gate characteristics, transistor parameters such as transistor widths, lengths, connected in device channel, etc. (Figs. 9, 14, col. 9, lines 15-50, col. 10, lines 12-57, for example). The design rule checker program is to check transistor noises such as transient noise, noise levels, etc. for noise immunity (cols. 9-12). Luk does not expressly disclose the claimed "gate width" of the gate transistors under rule checking (DRC) program.

Practitioner in the art at the time of the invention was made would have found Luk chip design verification above would include the claimed gate width because the design rule check program checks CMOS gate transistor layout which would include parameters such as transistor gate width, size, etc. in determination of noise immunity.

As per claim 9, Luk discloses the CMOS technology being used to design the logic gates. The gate includes p and n type transistor. Each transistor has a width and length as known in the art. By accessing the gate characteristics, the rule checker program executes program codes to verify the noise immunity of the related block gates (Fig. 14, col. 11, lines 6-25, and col. 12, lines 2-28) or other noises present in the circuit (col. 5, lines 5, lines 36-44, for example).

As per claim 15, Luk discloses a system and computer readable medium stored therein computer program codes to implement a design check rule program for compilation of the chip design to meet performance with feature limitations similar to the claimed invention (Summary of the Invention, col. 8, lines 33-38, for example). According to Luk, the rule checking program in the computer readable medium for design rule verification includes means or codes:

Configuring a computer to execute a rule checker program (Figs. 9, 14, col. 8, lines 33-53, col. 12, lines 21-28),

wherein the design rule being checked for noise performance of an integrated circuit design having CMOS gates, gate connected in datapath or along circuit paths including static gate characteristics, transistor parameters such as transistor widths, lengths, connected in device channel, etc. (Figs. 9, 14, col. 9, lines 15-50, col. 10, lines 12-57, for example). The design rule checker program is to check transistor noises such as transient noise, noise levels, etc. for noise immunity (cols. 9-12). Luk does not expressly disclose the claimed "gate width" of the gate transistors under rule checking (DRC) program.

Practitioner in the art at the time of the invention was made would have found Luk chip design verification above would include the claimed gate width because the design rule check program checks CMOS gate layout, wherein gate layout parameters include transistor gate width, size, etc. for the determination of noise immunity.

As per claim 16, Luk discloses the CMOS technology being used in the design of logic gates. The gate includes p and n type transistor. Each transistor has a width and length as known in the art. By accessing the gate characteristics such as transistor widths and lengths, the rule checker program can verify the noise immunity of the related block gates (Fig. 14, col. 11, lines 6-25, and col. 12, lines 2-28).

Allowable Subject Matter

3. Claims 3-7, 10-14, and 17-20 are objected to as being dependent upon rejected base claims, but would be allowable if rewritten in independent forms including all of the limitations of the base claims and any intervening claims.

Dependent claims 3-7, 10-14, and 17-20 are objected to because the claims require a plurality of checking models for rule checking program and method, each rule checking model is associated with ratio of the width of the P-field transistor to the width of the N-field transistor, the ratio corresponding to the numerical value stored in the memory device. In each checking model, the rule checker program obtaining a (first) ratio of the width of the n and p-type transistor of the first model, the first ratio used to access the first and second threshold values stored in the memory device, the rule checker program determines noise levels on the inputs taking possible high or low

values, and compares the determined noise levels to the first and second threshold values to determine the gate meets acceptable noise immunity requirement with respect to each model as claimed herein. The closest prior art of record does not expressly disclose such limitations as in the dependent claims

Response to Arguments

4. Applicant's arguments with respect to claims 1, 2, 8, 9, and 15-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Thai Phan whose telephone number is 571-272-3783. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached on 571-272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mar. 26, 2005

Thai Phan
Patent Examiner
Art Unit 2128